ACD Inputs to the DAQ Requirements Document (DRD)

Version 2 – incorporates comments from Steve and Jeff.

3.3 ACD Event Data

The ACD produces the following data:

- A logic signal when a minimum ionizing particle hits a tile = VETO
- A logic signal when a highly ionizing particle (e.g. Carbon, Nitrogen or Oxygen) hits a tile = CNO
- A 12-bit pulse height analysis (PHA) value for each tile upon receipt of a L1T signal.
- Miscellaneous housekeeping data (rates, voltages, temperatures, command verification, thresholds)

The following sections describe how these signals are used.

3.3.1 VETO

3.3.1.1 Fast (hardware) VETO

This signal offers the possibility of using the ACD in the hardware trigger.

- Supertile VETO signals for each tower are formed in the ACD electronics by an “and” of VETO signals from the nearest neighbor tiles to a tower.
- The supertile VETO signals are carried by dedicated wires to each tower

3.3.1.2 Slow (logic) VETO

This is the default mode for using the ACD veto signals.

- A 145 bit VETO word is formed with each L1T (therefore, the rate is the same as L1T, 1 - 10 Khz)
- A set bit in the word indicates a charged particle passing through a given tile
- This word is needed after every L1T for the next level of processing
- The 145 bit VETO word is sent to all towers
• The 145 bit VETO word should be included with event data for each event transmitted

3.3.2 CNO

The calorimeter will use heavy charged particle cosmic rays as a calibration source. The ACD CNO signal is used to override the ACD veto of these events and, if necessary, to alert the calorimeter readout system in case a different readout mode is desired.

• A 145 bit CNO word is formed with each L1T (therefore, the rate is the same as L1T, 1 - 10 Khz)
• A set bit in the word indicates a highly-ionizing charged particle passing through a given tile
• This word is needed after every L1T for the next level of processing
• The 145 bit CNO word is sent to all towers
• The 145 bit CNO word should be included with event data for each event transmitted

3.3.3 PHA

• A 12-bit pulse height analysis (PHA) word is constructed for each of the 145 tiles for each L1T
• Two bits are added to this word – one is set if the VETO is triggered for the tile, one is set if the CNO is triggered for the tile
• The purpose of the PHA is performance verification for the ACD threshold settings, not for use in the trigger

4. Science Housekeeping

4.1.3 ACD Science Housekeeping

4.1.3.1 Rates

The following rates should be accumulated continuously and transmitted to the ground ~ once per second:

• Veto rate for each of the 145 tiles
• CNO rate for each of the 145 tiles
• Supertile rate for each of the 16 towers

4.1.3.2 PHA Histograms

These histograms are used to confirm the threshold settings for the VETO and CNO discriminators.

Two modes (selectable by command):

• 2 histograms for each tile accumulated on-board for each of the 145 tiles, transmitted periodically with housekeeping
  1. PHA values when VETO is set
  2. PHA values when CNO is set
• Individual PHA values (one for each tile) sent with each L1T

5. Commanding

5.3 ACD Commanding

The following discrete commands are required:

• Power on/off for each phototube (2 x 145)
• Power on/off for each ACD electronics box (2)

The following analog commands are required:

• HV setting for each phototube (2 x 145) or each group of phototubes
• Veto threshold setting for each tile (145)
• CNO threshold setting for each tile (145)
• PHA threshold setting for each tile (145)
• Readout of command verification for each command is needed. These can be read out infrequently, ~ once per minute.
• Reprogramming of the supertile pattern
• Reprogramming of the “any X tiles” test in the supertile veto.

• Selection of PHA data transmission mode – histograms or individual values

6. Instrument Health and Other Housekeeping

The following housekeeping parameters should be read out periodically (~ once per minute) for each of the 145 tiles:

<table>
<thead>
<tr>
<th>Analog Signal</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0 VREF</td>
<td>Voltage reference for the analog circuit</td>
</tr>
<tr>
<td>1 PHA_VREF</td>
<td>Voltage reference used for the PHA</td>
</tr>
<tr>
<td>2 PREAMP_X10</td>
<td>PREAMPOUT multiplied by a factor of ten</td>
</tr>
<tr>
<td>3 PREAMPOUT</td>
<td>Diagnostic point after the first amplifier</td>
</tr>
<tr>
<td>4 PHA_DISCR_THR</td>
<td>PHA threshold</td>
</tr>
<tr>
<td>5 HIGH_DISCR_THRESH</td>
<td>CNO threshold</td>
</tr>
<tr>
<td>6 DIS_THRESH</td>
<td>VETO threshold</td>
</tr>
<tr>
<td>7 SPARE 1</td>
<td>TBD</td>
</tr>
<tr>
<td>8 SPARE 2</td>
<td>TBD</td>
</tr>
<tr>
<td>9 TEMP_HOT</td>
<td>Hottest temperature in the channel</td>
</tr>
<tr>
<td>10 TEMP_VREF</td>
<td>Temperature of the voltage reference</td>
</tr>
<tr>
<td>11 HV_IMON</td>
<td>Current associated with the high voltage line.</td>
</tr>
<tr>
<td>12 HV_CMD_DAC</td>
<td>Command to the power supply</td>
</tr>
<tr>
<td>13 HV_MON</td>
<td>High voltage (only one value per GSFC FPGA)</td>
</tr>
<tr>
<td>14 PHA_FOLLOW</td>
<td>PHA_ACD_IN + 2.5V + 40%</td>
</tr>
<tr>
<td>15 PHA_ACD_IN</td>
<td>PHA AD converter input backup</td>
</tr>
</tbody>
</table>

If the phototubes have individual HV converters, then a HV readout is needed for each phototube rather than each tile.
8. Instrument Support

8.1.3 ACD Diagnostic Mode

The purpose of this mode is to detect and isolate problems in the single tile electronics chains. It **should** be done autonomously, on-board, with sufficient flexibility to correct problems.

Requirements:

- Software **must** control connections between the pairs of phototubes attached to a single tile
- Counters with adequate resolution
- Code to selectively isolate components, run tests and evaluate results

8.3 Power Distribution and Management

8.3.3 ACD Power

The +28 V needed by the ACD **will** be supplied through the DAQ. HV **will** be generated within the ACD system. Other voltages TBD.

9. I&T Support

Because the ACD **will** be assembled and tested as a unit separate from the towers, it is essential that a DAQ simulator be available early in the assembly process.

Requirements:

- FPGA representing the L1T input – in order to verify timing of hardware VETO signal
- TEM representing data bus – in order to verify transmission of event and housekeeping data
- Software to display: all count rates, all housekeeping values, all command verification, both modes of PHA readout.
- Software to interpret mnemonics and transmit commands to the ACD